What is claimed is:

1. A logical equivalence verifying device for performing logical equivalence verification of two prescribed circuits to display the results thereof, said device comprising:

a first identifier recording section that performs structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and records each result of said structural matching as an identifier for each element;

a subcone extracting section that extracts a plurality of collections of elements as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

a verifying section that verifies logical equivalence between said two circuits for each subcone extracted by said subcone extracting section; and

a display control section that displays a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

2. A logical equivalence verifying device for performing logical equivalence verification of two prescribed circuits to display the results thereof, said device comprising:

a second identifier recording section that performs instance name matching for each element in which it is determined whether instance names of elements in corresponding logic cones of said two circuits match each other, and records the results of said instance name matching as identifiers, respectively;

a subcone extracting section that extracts a plurality of element collections as subcones from each of said logic cones, each element collection

including elements which are connected with each other and have the same identifier;

a verifying section that verifies logical equivalence between said two circuits for each subcone extracted by said subcone extracting section; and

a display control section that displays a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

3. A logical equivalence verifying device for performing logical equivalence verification of two prescribed circuits to display the results thereof, said device comprising:

a subcone extracting section that extracts subcones from corresponding logic cones of said two circuits by excluding prescribed portions of said logic cones by providing an external input to each of said prescribed portions to make their output to be at a constant value;

a verifying section that verifies logical equivalence between said two circuits for each subcone extracted by said subcone extracting section; and

a display control section that displays a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

4. The logical equivalence verifying device according to claim 3, wherein when said logic cone is divided into a plurality of portions by said prescribed portions, said subcone extracting section extracts said plurality of portions as subcones.

5. A logical equivalence verifying device for performing logical equivalence verification of two prescribed circuits to display the results thereof,

said device comprising:

an internal verification point associating section that selects internal verification points in corresponding logic cones of said two circuits, respectively, to observe outputs of portions thereof, and associates said internal verification points of one of said circuits with those of the other circuit;

a subcone extracting section that extracts subcones from said logic cones by using said internal verification points;

a verifying section that verifies logical equivalence between said two circuits for each subcone extracted by said subcone extracting section; and

a display control section that displays a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

6. The logical equivalence verifying device according to claim 1, wherein said display control section displays, based on the results of said logical equivalence verification, only those subcones for which said logical equivalence verification has resulted in mismatch.

7. A logical equivalence verifying device for analyzing causes of logical mismatch when a plurality of mismatched logic cones are detected which are logically mismatched logic cones as a result of logical equivalence verification between two prescribed circuits, said device comprising:

a storage section that stores elements constituting said mismatched logic cones;

an analyzing section that extracts, as analysis elements among said mismatched logic cones, those elements which constitute logic cones that have been selected as objects for analysis, further extracts, as pertinent logic cones, said mismatched logic cones including said analysis elements for each of said analysis elements, and calculates the number of said pertinent logic cones as a pertinent number for each of said analysis elements; and

a display control section that displays said pertinent number for each of said analysis elements.

8. The logical equivalence verifying device according to claim 7, wherein said display control section displays only those of said analysis elements for which said pertinent number is within a prescribed range.

9. The logical equivalence verifying device according to claim 7, wherein said display control section further displays an identifier of each of said pertinent logic cones for each of said analysis elements.

10. The logical equivalence verifying device according to claim 7, wherein said display control section highlights those output points which are subject to influences due to a correction of elements.

11. The logical equivalence verifying device according to claim 7, wherein said display control section highlights those output points which are subject to influences due to a constraint of an input for excluding a prescribed portion not to be verified.

12. The logical equivalence verifying device according to claim 1, wherein said two prescribed circuits comprise a pre-change one and a post-change one of a circuit being designed when said circuit is changed.

13. A logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

a step for performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

a step for extracting a plurality of element collections as subcones from

each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

a step for performing logical equivalence verification between said two circuits for each of said subcones; and

a step for displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

14. A logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said device comprising:

a step for performing instance name matching for each element in which it is determined whether instance names of elements in corresponding logic cones of said two circuits match each other, and recording the results of said instance name matching as identifiers, respectively;

a step for extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

a step for performing logical equivalence verification between said two circuits for each of said subcones; and

a step for displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

15. A logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

a step for extracting subcones from corresponding logic cones of said

two circuits by excluding prescribed portions of said logic cones by providing an external input to each of said prescribed portions to make their output to be at a constant value;

a step for performing logical equivalence verification between said two circuits for each of said subcones; and

a step for displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

16. A logical equivalence verifying method for performing logical equivalence verification of two prescribed circuits to display the results thereof, said method comprising:

a step for selecting internal verification points in corresponding logic cones of said two circuits, respectively, to observe outputs of portions thereof, and associating said internal verification points of one of said circuits with those of the other circuit;

a step for extracting subcones from said logic cones by using said internal verification points;

a step for performing logical equivalence verification between said two circuits for each of said subcones; and

a step for displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

17. A logical equivalence verifying method for analyzing causes of logical mismatch when a plurality of mismatched logic cones are detected which are logically mismatched logic cones as a result of logical equivalence verification between two prescribed circuits, said method comprising:

a step for storing elements constituting said mismatched logic cones;

a step for extracting, as analysis elements among said mismatched logic cones, those elements which constitute logic cones that have been selected as objects for analysis, further extracting, as pertinent logic cones, said mismatched logic cones including said analysis elements for each of said analysis elements, and calculating the number of said pertinent logic cones as a pertinent number for each of said analysis elements; and

a step for displaying said pertinent number for each of said analysis elements.

18. A logical equivalence verifying program for making a computer execute a logical equivalence verifying method which performs logical equivalence verification of two prescribed circuits to display the results thereof, said program adapted to make said computer execute the steps of:

performing structural matching in which it is determined whether there are those portions in corresponding logic cones of said two circuits which correspond in circuit structure to each other, and recording the results of said structural matching as an identifier for each element;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

19. A logical equivalence verifying program for making a computer execute a logical equivalence verifying method which performs logical equivalence verification of two prescribed circuits to display the results thereof, said program

adapted to make said computer execute the steps of:

performing instance name matching for each element in which it is determined whether instance names of elements in corresponding logic cones of said two circuits match each other, and recording the results of said instance name matching as identifiers, respectively;

extracting a plurality of element collections as subcones from each of said logic cones, each element collection including elements which are connected with each other and have the same identifier;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

20. A logical equivalence verifying program for making a computer execute a logical equivalence verifying method which performs logical equivalence verification of two prescribed circuits to display the results thereof, said program adapted to make said computer execute the steps of:

extracting subcones from corresponding logic cones of said two circuits by excluding prescribed portions of said logic cones by providing an external input to each of said prescribed portions to make their output to be at a constant value;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

21. A logical equivalence verifying program for making a computer execute a logical equivalence verifying method which performs logical equivalence verification of two prescribed circuits to display the results thereof, said program adapted to make said computer execute the steps of:

selecting internal verification points in corresponding logic cones of said two circuits, respectively, to observe outputs of portions thereof, and associating said internal verification points of one of said circuits with those of the other circuit;

extracting subcones from said logic cones by using said internal verification points;

performing logical equivalence verification between said two circuits for each of said subcones; and

displaying a first group of subcones with mismatched results of said logical equivalence verification and a second group of subcones with matched results of said logical equivalence verification while distinguishing between these first and second groups of subcones based on the results of said logical equivalence verification.

22. A logical equivalence verifying program for making a computer execute a logical equivalence verifying method for analyzing causes of logical mismatch when a plurality of mismatched logic cones are detected which are logically mismatched logic cones as a result of logical equivalence verification between two prescribed circuits, said program adapted to make said computer execute the steps of:

storing elements constituting said mismatched logic cones;

extracting, as analysis elements among said mismatched logic cones, those elements which constitute logic cones that have been selected as objects for analysis, further extracting, as pertinent logic cones, said mismatched logic cones including said analysis elements for each of said analysis elements, and calculating the number of said pertinent logic cones as a pertinent number for each of said analysis elements; and

displaying said pertinent number for each of said analysis elements.